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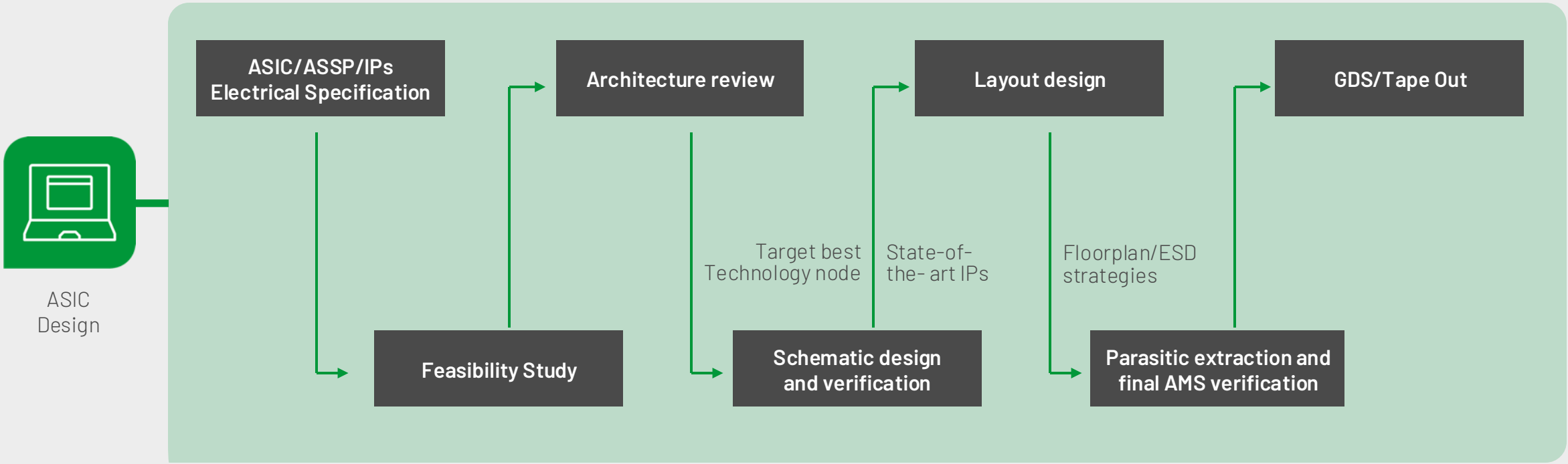
ASIC Design

2025

ICs / IPs design flow

INTEGRATED CIRCUITS (ICs) OR STAND-ALONE MACRO CELLS DESIGN (IPs)



Italian Fabless Company for IC development & industrialization

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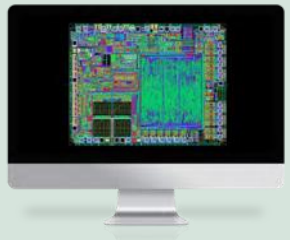
Design

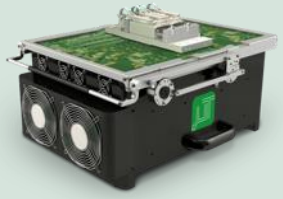


Layout

Characterization

Schematic

Qualification



DMT EVO

Ovenless Burn-In

Mass production

Celsius Evo Handler

Hatina GP

The scale of the ratio of the measurements in the representation do not correspond to the real one

DESIGN Expertise

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Analog Design

Digital Design

Silicon Layout

Analog design

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DEDICATED TO STATE-OF-THE-ART MACRO CELLS IPs

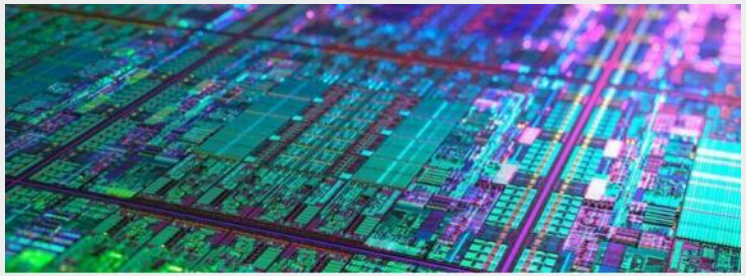
- **Analog domain** expertise is based on 20+ years of proven successful design in analog front-end
- **Analog mixed mode and mixed signal modeling and verification** skills for analog + digital characterization and verifications
- World-class expertise in analog front-end design, with a strong specialization in **Power Management** applications
- Experienced ICs design for **Consumer**, **Mobile and Automotive applications**
- **Analog ICs/IPs Layout design** deep expertise in CMOS/BCD/BiCMOS Technology nodes from 350nm down to 22nm

Analog Design | **Digital Design** | **Silicon Layout**

Power Management

POWER MANAGEMENT (PM) IP EXPERTISE

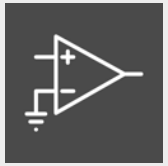
- Long-standing experience in **Power Management Applications**
- From **Low voltage** to **High voltage applications** (1.0V to 100V main voltage domains), **extremely low power** consumption, **high efficiency** design
- **Extensive portfolio** of PM IPs in a wide range of technology nodes, with silicon proven products results
- Deep understanding of **Mobile/Portable Devices** and **Automotive** application requirements
- **Modular approach** for easy porting, reducing risk and time to market



Analog Design | **Digital Design** | **Silicon Layout**

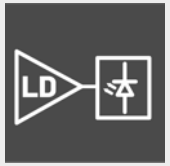
Analog Design expertise

High Accuracy
Voltage and Current
References



Voltage / Current /
Temperature Monitoring,
I/O Buffer, Oscillators, Comparators,
Operational amplifiers

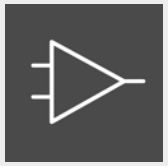
Trimming Structures
(antifuse, fuse, zener
zap methodology)



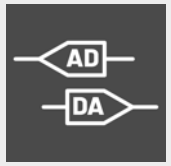
LED Drivers

High Efficiency
Charge pump

Battery chargers



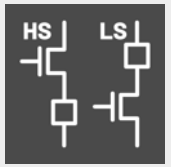
I/O Buffer, Oscillators,
Comparators,
Operational amplifiers



AD/DA Converters

Sensor interfaces
(DSI3-PSI5)

High-Low Side Drivers
(for valve, lamp,
injector, motor relay)



High-Low Side Drivers
(for valve, lamp,
injector, motor relay)

Linear and Switching
Voltage Regulators (LDOs
and DC/DC Converter)

Analog Design | **Digital Design** | **Silicon Layout**

Design for X

DESIGN FOR...

- ...Testability
- ...EMC
- ...Reliability
- ...Yield
- ...ESD Robustness
- ...Safety
- ...Quality

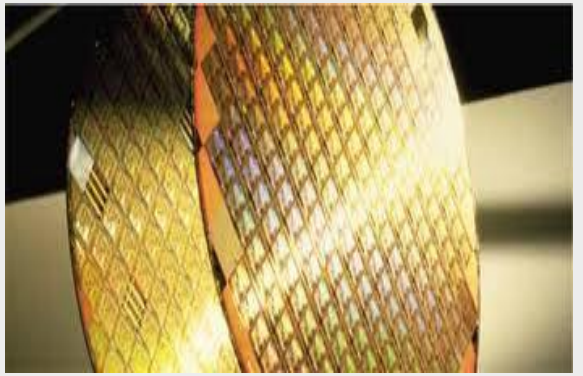
- Test Mode & Scan Pattern implementation
- Electromagnetic Compatibility (Emission & Immunity)
- Design Failure Mode and Effect Analysis
- Gate & Drain Stress, SHOVE, VLV & IDDQ Test to screen oxide & vias defects

Design for X

PRODUCT REALIZATION: DESIGN FOR TESTABILITY

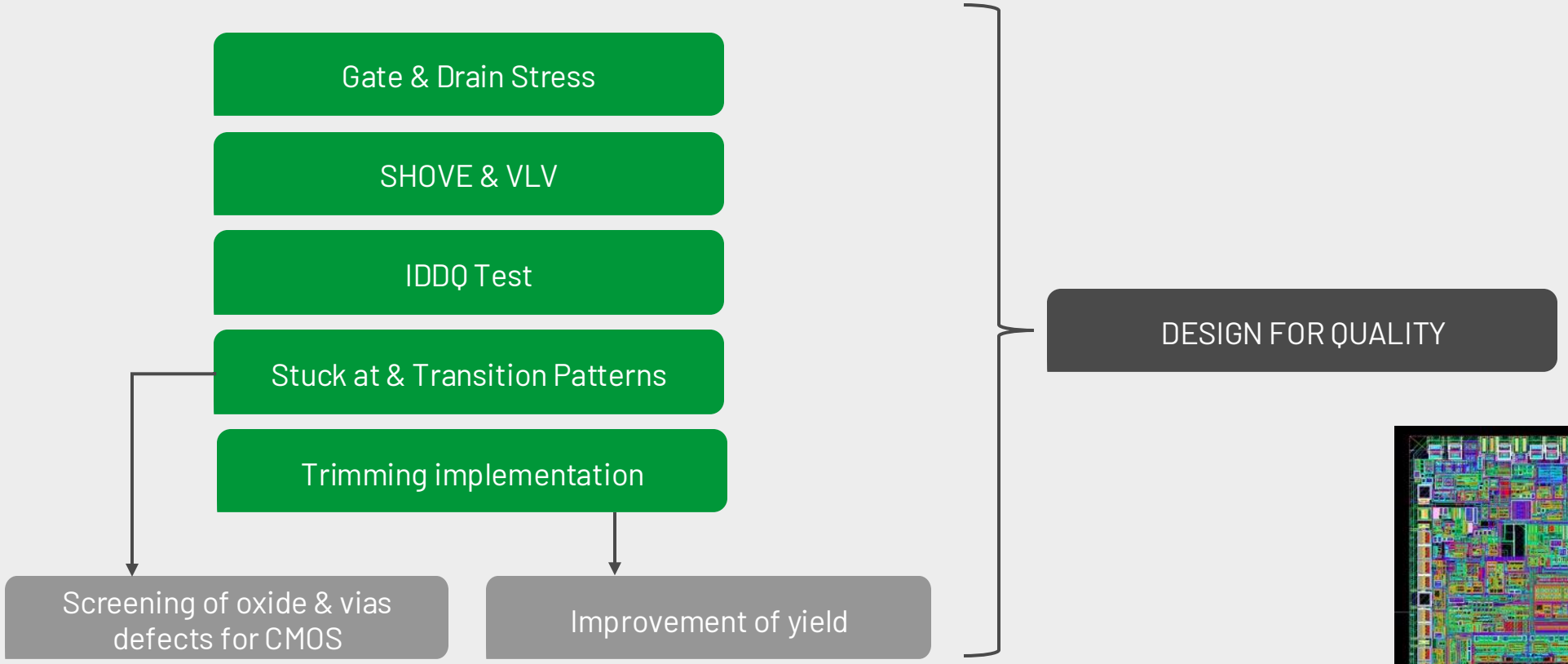
- Scan Pattern for a complete logic coverage
- Trimming implementation
- Observability of the analog functions (Test point access)
- Test mode procedure
- Test time reduction
- External control for analog & digital functionalities
- Quality test Implementation

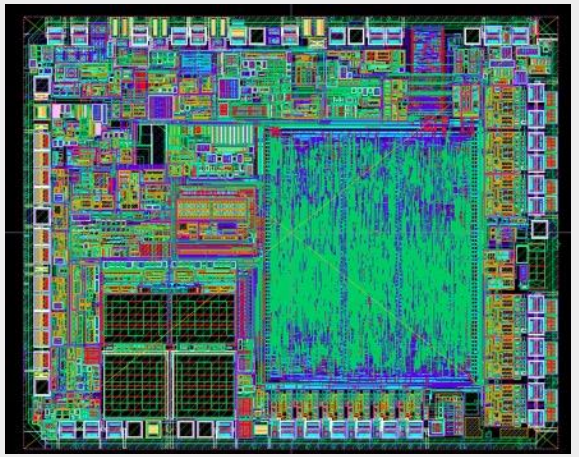
→ DESIGN FOR TESTABILITY → Cost saving & Quality Improvement



Design for X

PRODUCT REALIZATION: DESIGN FOR QUALITY



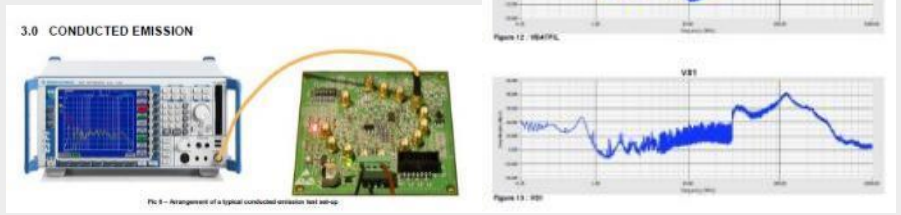


Design for X

PRODUCT REALIZATION: DESIGN FOR X

- Design oriented to avoid NBTI / PBTI effects
- ISO9637 Robustness
- ESD Robustness (HBM, MM, CDM)
- Latch-up Robustness
- Electromagnetic Compatibility (Conducted Emission, Immunity
- Potential Failure Analysis of Safety Functionalities (ISO26262)

- DESIGN FOR RELIABILITY
- DESIGN FOR YELD
- DESIGN FOR ESD/LU, EMC
- DESIGN FOR SAFETY

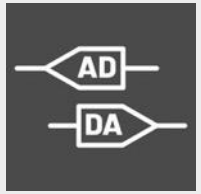


Digital Design

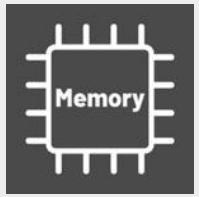
Fitting and programming of FPGA Xilinx

Serial Interface
UART | SPI | I2C | CAN-bus Interface | LIN-bus Interface | DSI3 Interface | PSI5 Interface

Diagnostic
Temperature | Current Voltage | Watchdog



Converter interface
DAC | ADC

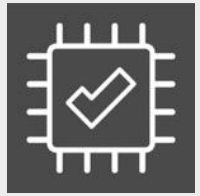


Memory Interface
NVM | RAM | OTP

Regulator Interface
DCDC | Linear

Signal processing
Digital filter | FFT | AVG PID | Clock generator PWM generator

Multidomain clocks and supplies
Handshake protocol



DFT

SYN – ATPG - LBIST

Layout
Formality | STA | Power Integrity | PLS

ADMS

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Silicon Layout

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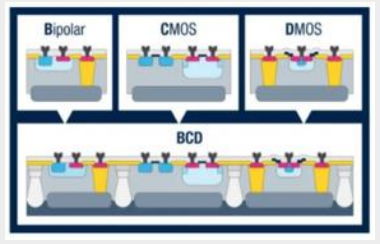
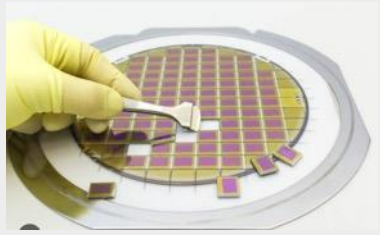
Silicon Layout Expertise

Physical layout implementation from single IP to full custom IC, covering various technologies, such as:

- ATMEL Standard and High Voltage CMOS 0.18/0.35 mm, Embedded Non Volatile Memory
- ST Standard CMOS 0.18/0.35 mm, BCD 0.18/0.35 mm (BCD6/BCD8/BCD9)
- Infineon CMOS 0.13/0.35 mm High Voltage (C9/C11HV)
- XFAB CMOS 0.18/0.35 mm
- TSMC CMOS 0.18/0.13 mm / BCD 55nm
- UMC CMOS 90 nm
- Texas Instruments BiCMOS 0.35 mm (LBC7/LBC8/LBC9)
- Dongbu HiTek CMOS/BCD High Voltage 110nm/130nm





Analog Design | Digital Design | Silicon Layout

Business models

FLEXIBLE BUSINESS MODELS ARE AVAILABLE

Baseline models

- Fixed Price
- Time & Material
- A combination of two previous models

Project Organization

- Program/Project Managers to be identified in both parties
- Single work location or multi-sites
- Project management according to customer security standard

Design/Simulation Platform used

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cadence®

Design/Layout Platform

- Design Virtuoso Schematic Editor XL
- Layout Virtuoso Layout Suite XL
- Calibre for LVS/DRC
- Tetramax (pattern ATPG)
- Innovus Cadence (Layout)

SYNOPSYS®

Digital Platform

- Synopsys Design Compiler
- Synopsys Test Compiler (Scan insertion)
- Synopsys PrimeTime (STA)

Mentor® A Siemens Business

A/D Simulation Platform

- EldoD Mentor
- ADMS Mentor
- Spectre SImulator
- Ezwave
- Cadence Incisive


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THANK YOU